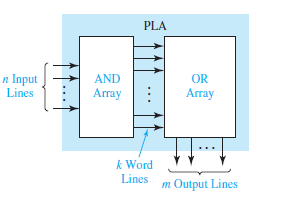
**Programmable Logic Devices**

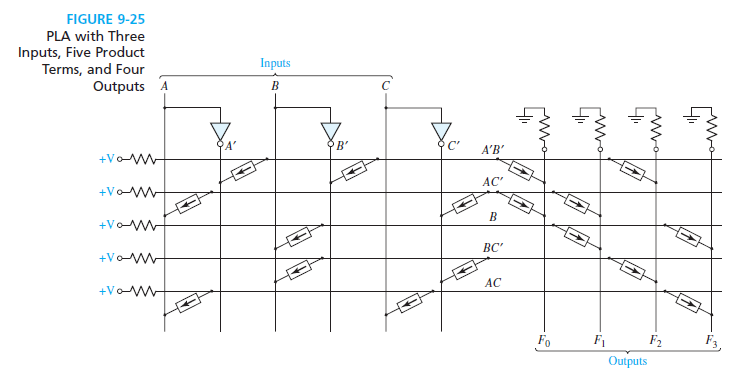
* A programmable logic device (or PLD) is a general name for a digital integrated circuit capable of being programmed to provide a variety of different logic functions.
* Simple combinational PLDs are capable of realizing from 2 to 10 functions of 4 to 16 variables with a single integrated circuit.
* More complex PLDs may contain thousands of gates and flip-flops.
* A single PLD can replace a large number of integrated circuits, and this leads to lower cost designs.
* When a digital system is designed using a PLD, changes in the design can easily be made by changing the programming of the PLD without having to change the wiring in the system.

**1. Programmable Logic Arrays**

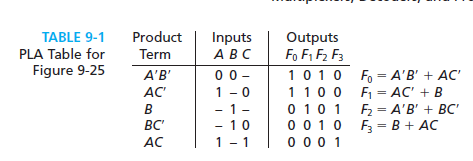
* A PLA with *n* inputs and *m* outputs can realize *m* functions of *n* variables



* An AND array which realizes selected product terms of the input variables.
* The OR array ORs together the product terms needed to form the output functions.
* A PLA implements a sum-of-products expression.



* Product terms are formed in the AND array by connecting switching elements at appropriate points in the array. For example, to form *AB*, switching elements are used to connect the first word line with the *A* and *B* lines.
* Switching elements are connected in the OR array to select the product terms needed for the output functions. For example, because *F*0 = *A’B*’+ *AC’*, switching elements are used to connect the *A’B’* and *AC’* lines to the *F*0 line.
* The contents of a PLA can be specified by a PLA table.
* The input side of the table specifies the product terms.
* The symbols 0, l, and – indicate whether a variable is complemented, not complemented, or not present in the corresponding product term.
* The output side of the table specifies which product terms appear in each output function. A 1 or 0 indicates whether a given product term is present or not present in the corresponding output function.

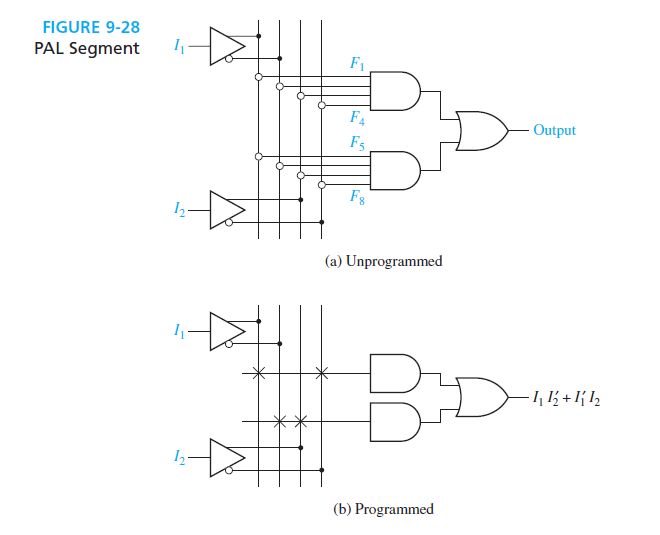


* There are 2 types:
* The mask-programmable type is programmed at the time of manufacture.
* The field-programmable logic array (FPLA) has programmable interconnection points that use electronic charges to store a pattern in the AND and OR arrays.

**2. Programmable Array Logic**

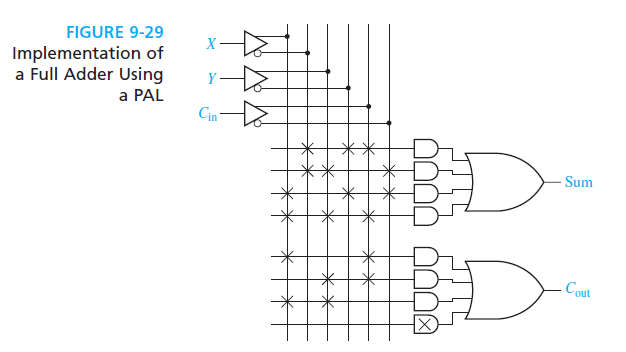
* The PAL (programmable array logic) is a special case of the programmable logic array in which the AND array is programmable and the OR array is fixed.
* Because only the AND array is programmable, the PAL is less expensive than the more general PLA, and the PAL is easier to program. For this reason, logic designers frequently use PALs to replace individual logic gates when several logic functions must be realized.
* Figure represents a segment of an unprogrammed PAL.
* A buffer is used because each PAL input must drive many AND gate inputs.
* When the PAL is programmed, some of the interconnection points are programmed to make the desired connections to the AND gate inputs.
* Connections to the AND gate inputs in a PAL are represented by X’s.

Eg:



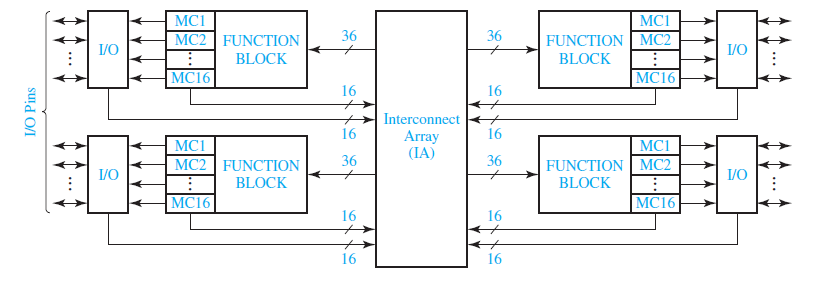
Eg2: Implement a full adder using PAL





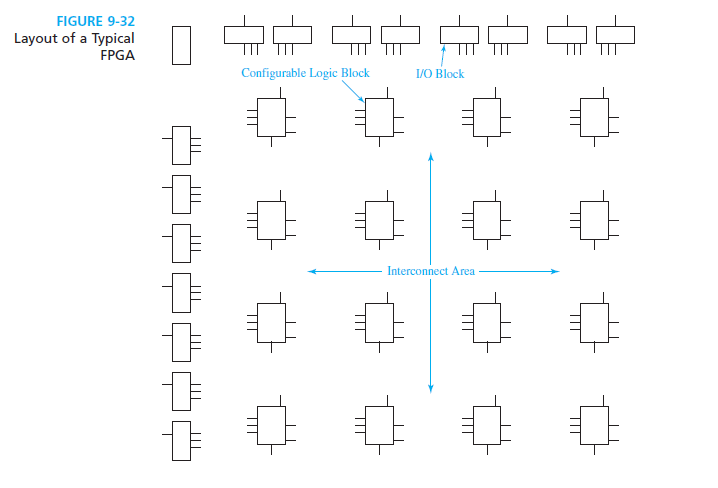
**Complex Programmable Logic Devices**

* Many PALs or PLAs can be placed on a single CPLD chip and interconnected.
* When storage elements such as flip-flops are also included on the same IC, a small digital system can be implemented with a single CPLD.
* Figure shows the basic architecture of a Xilinx XCR3064XL CPLD.
* This CPLD has four function blocks, and each block has 16 associated macrocells (MC1, MC2, .).
* Each function block is a programmable AND-OR array that is configured as a PLA.
* Each macrocell contains a flip-flop and multiplexers that route signals from the function block to the input-output (I/O) block or to the interconnect array (IA).
* The IA selects signals from the macrocell outputs or I/O blocks and connects them back to function block inputs. Thus, a signal generated in one function block can be used as an input to any other function block.
* The I/O blocks provide an interface between the bi-directional I/O pins on the IC and the interior of the CPLD.



**Field-Programmable Gate Arrays**

* An FPGA is an IC that contains an array of identical logic cells with programmable interconnections.
* The user can program the functions realized by each logic cell and the connections between the cells.
* Figure shows the layout of part of a typical FPGA.



* The interior of the FPGA consists of an array of logic cells, also called configurable logic blocks (CLBs).
* The array of CLBs is surrounded by a ring of input-output interface blocks.
* These I/O blocks connect the CLB signals to IC pins.
* The space between the CLBs is used to route connections between the CLB outputs and inputs.